AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application. Please amend the claims, as follows:

1-24 (Canceled)

25. (Currently Amended) An arrangement for generating addresses for interleaving/de-interleaving sequences ~~($x_1, x_2, x_3, .., x_K$)~~ including a given number (K) of items, the value of said given number of items (K) being within a given range of possible values, the arrangement comprising:

~~at least one~~ a first memory unit having stored therein a plurality of records, each record being indicative of a respective set of interleaving/deinterleaving parameters ~~(R, C, p, v)~~ for constructing a matrix for arranging said sequences and for affecting intra-row and inter-row permutation of said matrix to generate a permuted output matrix for generating said addresses, wherein said memory unit has a number of said records stored therein that is less than the number of values in said given range of possible values, and each said record in said memory unit is identified by a respective pointer; and

a pointer retrieval circuit associated with said memory unit, said pointer retrieval circuit configured for generating for each value of said given number of items (K) in said given range a corresponding pointer pointing to a respective record in said memory unit. ~~corresponding to at least one value of said given number (K) of items and generated by said at least one value.~~

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Currently Amended) The arrangement of claim ~~28~~ 25, wherein said pointer retrieval circuit comprises:

a circuit ~~sensitive to~~ operating in dependence on said given number of items (K) to derive therefrom a set of most significant bits of said pointers; and

a ~~respective~~ second memory unit having stored therein the remaining, least significant bits of said pointers.

30. (Previously Presented) The arrangement of claim 29, wherein said circuit comprises:

a plurality of comparators to compare said given number of items (K) with a number of given thresholds, and

a logic unit for combining the outcome of the comparisons carried out in said comparators and deriving therefrom said set of most significant bits of said pointers.

31. (Currently Amended) The arrangement of claim ~~26~~ 25, wherein said ~~at least one~~first memory unit comprises, for each said record, at least one flag signal taking one

of a first and a second logical value, said flag being set at said second logical value when said given number of items (K) for the corresponding record is equal to the product of the number of rows (R) and the number of columns (C) in said matrix and said number of columns (C) in said matrix equals the value of the parameter ~~(P)~~ (p) used for said intra-row permutation plus 1.

32. (Currently Amended) The arrangement of claim ~~26~~ 25, further comprising arithmetic circuitry exempt from multipliers and dividers for generating a pseudo-random sequence of the type ~~(a*b mode c)~~ (a*b mod c) for producing a permutation pattern for use in said intra-row permutation.

33. (Currently Amended) The arrangement of claim ~~26~~ 25, further comprising first and second permutation modules for performing said intra-row and said inter-row permutations, said module for performing an inter-row permutation being arranged upstream of said module for performing intra-row permutation.

34. (Previously Presented) The arrangement of claim 33, comprising an intra-row module for producing a sequence (q) for performing said intra-row permutation, said intra-row module being configured for assigning $q_0 = 1$ to be the first prime integer in said sequence (q) and determining the prime integer q_i in the sequence to be a least prime integer such that the greatest common divisor $(qi, p - 1) = 1$, $q_i > 6$, and $q_i > q_{(i-1)}$ for each i = 1, 2, ..., R - 1.

35. (Previously Presented) The arrangement of claim 34, wherein said intra-row module comprises:

a prime numbers table for reading at least the prime integer therefrom; and

a look up table for managing the greatest common divisor operation.

36. (Currently Amended) A method of generating addresses for interleaving/de-interleaving sequences ~~$(x_1, x_2, x_3, ..., X_K)$~~ including a given number (K) of items, the value of said given number of items (K) being within a given range of possible values, the method comprising the steps of:

generating, on the basis of at least one value of said given number (K) of items, records indicative of a respective set of interleaving/de-interleaving parameters for constructing a matrix for arranging said sequences and affecting intra-row and inter-row permutation of said matrix to generate a permuted output matrix for generating said addresses; ~~(R, C, p, v); and~~

storing in ~~at least one~~ a first memory unit a number of said records that is less than the number of values in said given range of possible values; and ~~said set of interleaving/de-interleaving parameters (R, C, p, v).~~

identifying each said record in said memory unit by a respective pointer and generating for each value of said given number of items (K) in said given range a corresponding pointer pointing to a respective record in said memory unit.

37. (Canceled)

38. (Canceled)

39. (Canceled)

40. (Currently Amended) The method of claim ~~39~~ 36, comprising the steps of retrieving said pointers by:

deriving from said given number of items (K) a set of most significant bits of said pointers; and

storing the remaining, least significant bits of said pointers in a ~~respective~~ second memory unit.

41. (Previously Presented) The method of claim 40, comprising the steps of:

comparing said given number of items (K) with a number of given thresholds; and

combining the results of comparisons to derive therefrom said set of most significant bits of said pointers.

42. (Currently Amended) The method of claim ~~37~~ 36, comprising the step of storing, for each said record, at least one flag signal taking one of a first and a second logical value, said flag being set at said second logical value when said given number of items (K) for the corresponding record is equal to the product of the number of rows (R) and the number of columns (C) in said matrix and said number of columns (C) in said matrix equals the value of the parameter ~~(P)~~ (p) used for said intra-row permutation plus 1.

43. (Currently Amended) The method of claim ~~37~~ 36, comprising the step of generating a pseudo-random sequence of the type ~~(a*b mode c)~~ (a*b mod c) for producing a permutation pattern for use in said intra-row permutation, said generating step being carried out by means of a linear algorithm exempt from multiplications and divisions.

44. (Currently Amended) The method of claim ~~37~~ 36, wherein said inter-row permutation is performed before said intra-row permutation.

45. (Previously Presented) The method of claim 44, comprising the step of producing a sequence (q) for performing said intra-row permutation, said intra-row module being configured for assigning $q_0 = 1$ to be the first prime integer in said sequence (q) and determining the prime integer q_i in the sequence to be a least prime integer such that the greatest common divisor $(q_i, p - 1) = 1$, $q_i > 6$, and $q_i > q_{(i-1)}$ for each $i = 1, 2, ..., R - 1$.

46. (Currently Amended) A turbo encoder including at least one of an interleaver and a de-interleaver module, said at least one module including an arrangement for generating addresses according to claim 25 or any one of claims ~~25~~ 29 to 35.

47. (Currently Amended) ~~A computer program product directly loadable in the memory of a digital computer and including~~ A computer-readable medium configured to store instructions for execution by a processor in a digital computer, the instructions

including a software code portion for performing the method of claim 36 or any one of claims ~~36~~ 40 to 45. ~~when the product is capable of being run on a computer.~~

Please add new claim 48:

48. (New) A turbo decoder including at least one of an interleaver and a de-interleaver module, said at least one module including an arrangement for generating addresses according to claim 25 or any one of claims 29 to 35.